MATLAB Based Cost Modeling for VLSI Testing

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Abstract: The cost for testing integrated circuits and systems is growing rapidly as their complexity is increasing as per Moore’s law. Cost modeling plays a very vital role in reducing test cost and time to market. It also gives estimate of overall testing. The economics modeling for VLSI testing with Automatic Test Equipment (ATE) is presented in this paper. The mathematical relations are developed for cost model to test the VLSI circuits based on the parameters of ATE testing, further cost modeling equations are modeled into Graphical User Interface(GUI) in Matlab, which can be used as a cost estimation tool. A case study is done for Set-top-box, Microprocessor, Device A to verify the functionality of the developed estimation tool. It helps the Test engineers for estimating the testing cost for the test planning.

Index Terms—Cost Model, Automatic Test Equipment, Graphical User Interface, Design for Testability

1. INTRODUCTION

Test cost is very important factor for complex chip designs. As the trend of System on Chip appears in the industry, the Integrated circuit designs turn into more complex than the conventional designs, so the expense of testing is increased. The cost related to the development of semiconductor testing procedures and methods for ATE are the main driving factor. The mathematical algorithms or parametric equations used to estimate the costs of a product or project are known as cost estimation models. These models are typically essential for business plans/budgets, and other financial planning and tracking mechanisms. The continuing focus on cost of the test will result in a better understanding of cost trade-offs between test methodologies as per ITRS 2007[1] as shown in figure1. Typically, the cost of test boosts exponentially with an improvement in defects per million (DPM). Mathematical modeling in MATLAB GUI (graphic user interface) is very powerful as it reduces the designer’s time. Modification of any designed function in MATLAB GUI is very easy. The flexibility of MATLAB is used for rapid deployment of the complex software to the end user.
The paper is organized as follows: Section 2 describes the related work of economics of VLSI Testing and cost modeling. Section 3 presents the test cost model that is used for the automatic test equipment for multisite module testing. In Section 4 gives procedure for the cost modeling tool development using Matlab. Section 5 discusses a case study three devices for the verification of the economic analysis tool. The paper ends with the conclusions in Section 6.

2. RELATED WORK

Many researchers have explored the idea and benefits of the cost of manufacturing test in the past. Some of them are discussed here. Von-Kyoung Kim et. al.[3] proposed a test cost prediction model which estimates and optimize manufacturing test cost. I.D. Dear et.al.[2] the authors discussed the economics of test. The EVEREST test strategy planner tool, which is used for the test planning. Andrew[4]developed a Semiconductor Test Economic Model that can easily be applied to lowering overall cost of test and improving throughput. It gives idea to the Test Engineers for better decisions on the issues related to: test time reduction, multisite testing, yield, handler index time, ATE Utilization, and ATE purchasing. Erik et.al[5] discussed the benefits and tradeoffs by applying the technical cost modeling on 4 applications. Kenneth[6] gives the estimated the economic benefits of the DFT and also suggested that testability features should not be added to complex or high volume products. Abadir et al. [7] developed Hi-TEA, a MCM testing strategy selection tool, which helps to select the cost effective test strategy for the multi-chip module(MCM). Their tool required cost parameters such as die test cost and wafer yield, which are the parameters difficult to know in the early stage of design. Therefore, their tool may not be practical to predict a chip testing cost early on.
3. **Economic cost model for ATE based VLSI Testing**

The cost of semiconductor test to the organization has many drivers that are labor cost, floor space cost, Maintenance cost, ATE cost per site etc. The significance of these drivers varies substantially from one device to another. Test development costs are more important for the products with lower volume. Cost model is structured with the help of cost parameters figure 2.

![Figure 2: Economic cost model for ATE based VLSI Testing.](image)

The cost model is targeted the reduction of the capital equipment cost and the test time. The area overhead due to Design for Testability (DFT) implementation is not considered here so silicon overhead cost for DFT is not modeled. Therefore, this model considers only cost associated with spending time on equipment and test engineering. Cost model is used for wafer sorting during testing. One assumption is made here is that all functional tests are done in package test [10].

The cost is calculated as:

\[
C_t = \frac{C_{testcell} \cdot T_{total}}{N_{site}} \cdot \frac{N_p \cdot C_p}{N - N_{life-volume}} \tag{1}
\]

- \(C_{testcell}\) : Total capital equipment cost of the test cell,
- \(N_p\) : Number of Probe cards
- \(T_{total}\) : Total time a die spends on the equipment
- \(C_t\) : Total time of a die spends on the ATE
- \(N_{site}\) : Number of dies tested in parallel.
- \(C_{cap}\) : Constant consist amortization, utilization, labor cost, floor space, maintenance and training cost.
To calculate \( N_p \) equation is given as

\[
N_p = \left[ \frac{N_{\text{life-volume}}}{N_{\text{site}} + N_{\text{mtd}}} \right] \quad \text{2}
\]

where

- \( N_p \): No. of probe cards
- \( N_{\text{mtd}} \): Maximum touchdowns and
- \( N_{\text{life-volume}} \): Life time volume of dies

The cost of \( N_p \) probe cards, which cost \( N_{\text{life-volume}} \) of the product and maximum touchdowns \( N_{\text{mtd}} \). The pseudo code the developed cost model is given below:

```matlab
{Enter the required data from user like
Enter Probe card cost;
Enter number of devices ;}
First of all for the calculation of \( N_{\text{site}} \) Matlab code is
\( \text{Rsignal} = .1; \)
\( \text{Ns} = \text{str2double (a)}/\text{str2double (b)}; \)
\( \text{Ns } _\text{ATE}=\)
\( \text{str2double (c)}/ \text{str2double (d)}; \)
\( \text{if (Ns < Nsite } _\text{ATE}) \)
\( \text{Nsites } _\text{MS} = \text{Nsite } _\text{ms}; \)
\( \text{Else (Nsites } _\text{MS} = \text{Nsite } _\text{ms } _\text{ATE} ; \)
\( \text{end } ) \}
{Similarly Matab code is developed to calculate the total cost } C_t}
```

### 4. COST MODELING TOOL WITH MATLAB GRAPHICAL USER INTERFACE

Market modeling and Cost prediction/Estimation are new areas in which interest of physical and mathematical researchers is growing due to the stochastic nature of the financial processes. Constraining by this interest it becomes necessary to develop comprehensive software environment, which will use the same models for the simplification for quantitative analysis. The main advantage for such approach is that it provides rapid prototyping, high-quality visualization, and enhanced model testing to the end users.
GUI design is based on mathematical equations and user inputs. Graphical User Interface is designed in MATLAB (.fig file) and backend callback functions are called from GUI for each calculation. Development of GUI and its link with the database are shown in figure 3. In this, GUI has been created for mathematical equations. Numbers of input variables are set depending upon the equation to be designed. Property of every single component is set in the Property Inspector. A MATLAB code is written, which is generated by the callbacks of a particular push button. An event is created by clicking on push button for final result calculations, which causes the function of the button to be executed. A link is established between database which is created in excel file and GUI.

![Figure 3: Tool development of Cost Modeling in MATLAB GUI](image)

The model will help us evaluate the direct cost impacts of various values in the balanced scorecard, for the test processes. Using cost models, the relative effectiveness of two different test processes can be evaluated. To calculate the total cost of each test process, the user is required to enter the input data as per parameters required for estimation are shown in the figure 4.
Figure 4: A view of tool developed for VLSI test cost based on ATE.

5: CASE STUDY FOR VERIFICATION OF COST MODELING TOOL

In this Case study three applications are considered. Data are taken for verification of developed tool from [5] as shown in Table 1. First device is a Set Top Box (STB) with medium complexity of 1 million transistor, second a Microprocessor chip (µP) with 5 million of transistor complexity and also having high pin count, Third device “A” is taken with low volume of transistors i.e. 250 K only, which can be tested with one probe card only but more probe cards are needed for µP IC tests on ATE. This tool gives the individual testing cost of the all devices and comparison of three of those devices is demonstrates graphical form in same GUI.

Table I. Devices for cost modeling and parameter specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Application</th>
<th>Set-top-box</th>
<th>µP</th>
<th>Device A</th>
</tr>
</thead>
<tbody>
<tr>
<td>N_lifetime</td>
<td>Device: Lifetime volume [k]</td>
<td></td>
<td>1000</td>
<td>5000</td>
<td>250</td>
</tr>
<tr>
<td>G</td>
<td>Device: Number of logic gates [M]</td>
<td></td>
<td>2</td>
<td>20</td>
<td>6</td>
</tr>
<tr>
<td>f_max,chain</td>
<td>Device: Maximum scan chain frequency [MHz]</td>
<td></td>
<td>20</td>
<td>100</td>
<td>30</td>
</tr>
<tr>
<td>f_max,I/O</td>
<td>Device: Maximum I/O frequency for scan [MHz]</td>
<td></td>
<td>100</td>
<td>400</td>
<td>200</td>
</tr>
<tr>
<td>P_total</td>
<td>Device: Total number of device pads for wafer test</td>
<td></td>
<td>300</td>
<td>1000</td>
<td>400</td>
</tr>
<tr>
<td>t_fix</td>
<td>Time for DC+PLL+ Mixed-signal+ Mem [s]</td>
<td></td>
<td>6</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>C_ATE0</td>
<td>ATE: Cost zero channel [k$]</td>
<td></td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>C_site</td>
<td>ATE: Cost per site resource [k$]</td>
<td></td>
<td>25</td>
<td>60</td>
<td>25</td>
</tr>
<tr>
<td>P_max,ATE</td>
<td>ATE: Maximum number of channels</td>
<td></td>
<td>1000</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>f_max,ATE</td>
<td>ATE: Maximum ATE data channel frequency [MHz]</td>
<td></td>
<td>250</td>
<td>400</td>
<td>400</td>
</tr>
<tr>
<td>C_chan</td>
<td>ATE: Channel Cost High / Low [$]</td>
<td></td>
<td>1K/400</td>
<td>1K/400</td>
<td>1K/400</td>
</tr>
<tr>
<td>C_prober</td>
<td>Prober: Cost [k$]</td>
<td></td>
<td>350</td>
<td>350</td>
<td>350</td>
</tr>
<tr>
<td>t_index</td>
<td>Prober: Index time [s]</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>c_capital</td>
<td>Test cost per sec on MS [$]</td>
<td></td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
</tr>
<tr>
<td>c_volume</td>
<td>ATPG test data volume per gate [bits]</td>
<td></td>
<td>400</td>
<td>400</td>
<td>400</td>
</tr>
<tr>
<td>P_ctrl</td>
<td>Number of control signals</td>
<td></td>
<td>3</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>f_max,probecard</td>
<td>Probe card: Maximum frequency [MHz]</td>
<td></td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>P_max,probecard</td>
<td>Probe card: Maximum number of contacts</td>
<td></td>
<td>1000</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>C_probecard</td>
<td>Probe card: Cost [k$]</td>
<td></td>
<td>20</td>
<td>60</td>
<td>20(reusable)</td>
</tr>
<tr>
<td>N_max,touchdown ns</td>
<td>Probe card: Maximum number of touchdowns [k]</td>
<td></td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>R_testport</td>
<td>Test port [%]</td>
<td></td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
</tbody>
</table>
6. CONCLUSION

In this paper, a cost modeling tool for ATE based VLSI testing is presented. The mathematical equations are modeled using MATLAB GUI interface in which a Graphical interface is provided to the test engineers which is helpful to save the time in cost calculations and that GUI also compares the three devices at a time, which will give the exact estimation for the testing cost during VLSI testing process. This work can be also extend for DFT or without DFT based cost models in MATLAB for the future work. For the future work, we are developing GUI based cost-modeling tool for DFT, BIST, and SOC for web based application and standalone systems.

REFERENCES

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**Authors Bio brief**

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